REMARKS

Claims 1-8 and 11-13 are pending in this application. Claims 1, 5, and 11 to 13 are independent. Claims 11 to 13 are new. Claims 9 and 10 have been canceled.

Claim Rejection – 35 USC 102

Claims 9 and 10 have been rejected under 35 U.S.C. 102(b) as being anticipated by Hideaki (JP 2000-165244; filed with the IDS of November 30, 2001 and having applicant – Sharp Corp). By this amendment Applicant has canceled claims 9 and 10. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 USC 103

Claims 1-8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art disclosed in the present application and Tamai et al. (JP 09-068692; a priority document of U.S. Patent 6,160,533). Applicant respectfully traverses this rejection.

Summary of the Present Invention

The present invention is directed to a testing device and testing method for a semiconductor integrated circuit (e.g. driver 1 in Figures 5, 7A, 7B, 9A, 9B, 10A, and 10B). The semiconductor integrated circuit has a plurality of base power supply input terminals (V1 to V6), and a voltage generation circuit (13) including a Gamma correction resistance driver (8) and a plurality of DA

converters (2-1 to 2-m) producing **gradation output voltages**. The testing device includes a tester power supply (7), which supplies **voltages to the input terminals** of the semiconductor integrated circuit, and a comparator (e.g. 12-1 to 12-m in tester 70, Figure 2) for comparing the gradation output voltages and reference voltages.

In other words, the testing apparatus of the present invention is characterized with respect to its application of voltages by a tester power supply 7 (e.g., see Figures 7A and 7B) and its digital judgment of corresponding gradation output voltages by a comparator 12-1 to 12-m (see Figure 2).

Gradation level intervals, as **test objects**, are decided by setting of different voltages to be applied at the **base power supply input terminals** of the semiconductor integrated circuit. For example, as shown in Figure 7A, testing of a 10 V liquid crystal driver of 256 gradations is conducted by setting values of the base power supply input voltages at two values and only gradation levels between base power supply terminals V1 to V2 are tested at first (in this case, a gradation level interval as the test object is the gradation levels at and between voltages to base power supply input terminals V1 and V2). Based on those two values, the gradation levels included at an in between the base power supply terminals V1 to V2 (the gradation level interval) are provided as gradation output voltages having differences of about 200 mV (based on 10000 mV divided by the 51 gradation levels between V1 to V2). Such a potential difference is well within the accuracy of the comparators. Then, as shown in Figure 7B, gradation output voltage levels at and in between base power supply terminals V2 to V3 (i.e., another gradation level interval as another test object) are similarly tested. Testing of all gradation

levels is conducted in a similar fashion by changing the settings of the base power supply voltages sequentially.

The gradation level intervals are decided such that the judgment of the gradation output voltage by the semiconductor testing apparatus is a digital judgment. The testing device of the present invention improves over the known prior art devices through its setting of the base power supply voltages applied to the base voltage generation circuit such that each gradation output voltage can be judged as pass or fail (see Figure 8).

In order to aid in understanding the present invention as compared to the prior art testing devices, the following table is provided.

Power Supply Voltages: prior art vs embodiment of present invention

Input Terminal	Figure 5	Figure 7A
V1	10 volts	10 volts
V2	8	0
V3	6	0
V4	4	0
V5	2	0
V6	0	0

In the example shown in Figure 5, the gradation output voltage potential difference for each gradation level is about 40 mV (page 12, lines 1-6). In the example shown in Figure 7A, the potential difference is 200 mV (page 21, lines 1-6).

Disclosed Prior Art

The method of the present invention enables use of a simple and inexpensive comparator type tester (e.g., tester 70 shown in Figure 2) to be used with a gamma correction resistance type display driver (e.g., display driver 1 in Figure 5), i.e., that which produces a large number of gradations over multiple outputs. In conventional approaches based on a comparator, the potential difference between gradation levels was small such that a plurality of gradation levels existed between each judgment level (e.g., see Figure 3). Thus, it was impossible to determine the test accuracy for each gradation level.

On the other hand, the present invention includes a step of deciding "gradation level intervals" to be test objects. In other words, only gradation levels over an interval are to be tested as a test object. The gradation level interval can be decided such that there is a correspondence between the input gradation data signal of the semiconductor integrated circuit and the gradation output voltages such that testing of a gradation output voltage is a digital judgment (e.g., see Figure 8). The gradation level intervals, i.e. gradation levels to be tested, are established by setting different voltages to the base power supply input terminals of the semiconductor integrated being tested. Different voltages can be set such that a voltage to a base power supply input terminal is for one end of the gradation level interval and a base power supply input terminal is for the other end of the interval. Thus, unlike the prior art shown in figure 5, by using gradation level intervals as test objects the present invention can use a comparator type tester for testing a semiconductor integrated circuit having a large number of gradation levels over a plurality of outputs. Applicant submits that none of the disclosed prior art shows the deciding of "gradation level intervals" as test objects.

The Office Action relies on Figure 1 of the present disclosure for teaching the claimed "gradation level intervals to be test objects are decided by the setting of different voltages to be applied at the base power supply input terminals of said base voltage generation circuit." Applicant disagrees.

Prior art figure 1 shows gradation digital data equaling to the number of all output terminals m set beforehand, for every gradation level n, is sequentially input to the base power supply voltage input terminals 6-1 to 6-x (specification, page 3, lines 10-15). The voltage values for every gradation level are analog tested sequentially. The operation is repeated for all n gradations (specification, page 4, lines 1-7). Thus, Applicant submits that unlike the prior art figure 1, the present invention at least includes the step of deciding the gradation level intervals to be test objects.

The Office Action admits that the prior art disclosed in the present application fails to teach a step of assigning correspondence between the input gradation data signals of gradation levels of an interval, and the gradation output voltages. Instead, the Office Action relies on Tamai for teaching the deficiency. In particular, the Office Action states that Tamai's figures 4 and 13, and paragraphs 0005 and 0012 teach assigning correspondence between input gradation data signals and gradation output voltages. Applicant submits that the rejection has applied Tamai out of context and does not teach at least deciding gradation level intervals to be test objects.

Tamai teaches a driving method for a display panel and associated driving device. Tamai is silent with respect to testing of the driving device. Tamai's figure 4, for example, merely teaches a reference voltage source 42 for the source driver 37 (see Figure 1). Thus, unlike Tamai, in the

present invention by assigning correspondence between the input gradation data signals of the gradation levels of that interval, and the gradation output voltages, the gradation output voltage testing through the semiconductor testing apparatus is made to be a digital judgment. In the present claimed invention, the input gradation data signals are for gradation levels of the gradation level interval that is the test object. By assigning a correspondence between those input gradation data signals limited to a gradation level interval and gradation output voltages, the number of gradation levels of the test object are such that testing of a gradation output voltage is made by a digital judgment. Because Tamai is not concerned with testing of the display panel, it does not show the missing claimed method step.

Accordingly, Applicant submits that the rejection fails to establish *prima facie* obviousness for claim 1.

Claim 5 is directed to a testing device for semiconductor integrated circuits wherein a test object of the semiconductor integrated circuit is a gradation level interval, where different voltages are applied to the base power supply input terminal for the end of one side of the interval and a base power supply input terminal for the other end of the interval.

The Office Action admits that the prior art disclosed in the present application fails to disclose the claimed test object of the semiconductor integrated circuit. Instead, the Office Action relies on Tamai for making up for the deficiency. In particular, the Office Action relies on Tamai's figure 4 for teaching the claimed limitation.

Tamai's figure 4 merely teaches a reference voltage source for the source driver (e.g., in Tamai's figure 1, the reference voltage source 41 produces a single reference voltage 42 to the source driver 37; figure 4 produces a selected voltage as its output "out"). Tamai is silent with respect to testing of the source driver. Element 37 in Tamai might be considered a comparable semiconductor integrated circuit, but there is no testing system disclosed for that circuit. Thus, Tamai's figure 4 does not actually teach at least a gradation level interval being the test object.

Accordingly, Applicant submits that Tamai fails to make up for the deficiency in the applicant's disclosed prior art, and therefore the rejection fails to establish *prima facie* obviousness for claim 5.

New Claims

An important feature of the present invention is the setting of voltages applied to the input terminals of the driver device corresponding to a designated gradation level interval being a test object. In particular, the present invention is an improvement over the prior art shown in Figure 5, which resulted in an inability to use a comparator type tester as a testing device such as than shown in Figure 2.

Thus, new claims have been added that emphasize the key features of the present invention over that shown in Figure 5 in the present application and to cover the alternative embiments disclosed in present figures 9A, 9B, 10A, and 10B. In particular, claim 11 is comparable to original claim 5 with the difference that it explicitly defines a test object relative to a pair of base power

supply terminals. Claim 12 emphasizes the testing apparatus and a definition of test object. Claim 13 defines test object with respect to at least one less that all input terminals (e.g., Figures 10A and 10B). Claim 14 is an alternative method claim directed to steps shown in Figure 11.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-8 and 11-14 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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